REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the issues raised in the present Office Action, applicants acknowledge, with thanks, the Examiner's indication that Claims 24-35 are allowable and the Claims 8 and 9 would be allowable, if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Despite indicating that Claims 8 and 9 would be allowable if included within Claim 1, applicants have not amended Claim 1 to include those features. Instead, applicants have amended Claim 1 to positively recite that the claimed conductive interface has an upper surface that is in contact with said second semiconductor layer and a lower surface that is in contact with said first semiconductor layer. Support for this amendment to Claim 1 is found throughout the specification of the instant application. See particularly, FIG. 3 wherein reference numeral 14 is the conductive interface and reference numeral 16 is the second semiconductor layer, and reference numeral 12 is the first semiconductor layer. Applicants observe that the interface has upper and lower surfaces in the relationship with the semiconductor layers as presently claimed.

No further amendments to the remaining claims were made.

Claims 1 and 4-7 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Japanese Patent No. 2001068708 ("JP '708"), U.S. Patent No. 5,677,992 to Hayafuji, et al. ("Hayafuji, et al.") and U.S. Patent No. 6,759,277 to Flores, et al. ("Flores, et al.").

Applicants respectfully submit that Claims 1 and 4-7 are not rendered obvious by the combined disclosures of JP '708, Hayafuji, et al. and Flores, et al. since the combined prior art references do not teach or suggest applicants' claimed structure. Specifically, the combined disclosures of JP '708, Hayafuji, et al. and Flores, et al. do not teach or suggest applicants' claimed hybrid substrate including a first semiconductor layer having a first crystallographic orientation, and a second semiconductor layer having a second crystallographic orientation which is different from the first crystallographic orientation, wherein said first and second semiconductor layers are separated from each other by a conductive interface that has an upper surface that is in contact with said second semiconductor layer and a lower surface that is in contact with said first semiconductor layer, said conductive interface comprises a hydrophilic surface or a hydrophobic surface of at least one of said semiconductor layers.

JP '708 discloses a structure having different semiconductor layers of different crystal orientation one on top of another. JP '708 does not disclose that a conductive interface is present between the two semiconductor layers, let alone that the conductive interface has upper and lower surfaces that is in contact with the semiconductor layers as presently claimed.

Hayafuji, et al. disclose structures having semiconductor layers of different crystal orientation wherein a plurality of cladding layers, which may be conductive, are located therebetween. The applied secondary reference, however, does not teach or suggest applicants' claimed conductive interface that has an upper surface that is in contact with said second semiconductor layer and a lower surface that is in contact with said first semiconductor layer.

Flores, et al. provide an array of silicon dies on a substrate. The basic structure is shown in FIG. 1 wherein 106 is the substrate and 102 is the die which are joined together at surfaces 108 and 110. Applicants observe that the die 102 is comprised of Si and that the substrate 106 is a flexible or transparent substrate such as glass or a plastic. The applied reference (See FIG. 13) discloses that the wafer layer (i.e., die) is made hydrophilic and then it is attached to a flexible or transparent substrate. The applied reference does not teach or suggest the claimed hybrid substrate including two semiconductor layers of different crystal orientations that are separated by a conductive interface. Applicants observe that there is no mention in the prior art that the flexible or transparent substrate is a semiconductor and that is has a different crystal orientation from that of the die.

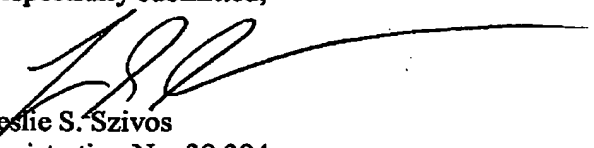
As such, the combined disclosures of JP '708, Hayafuji, et al. and Flores, et al. do not render the claims of the present application unpatentable.

The § 103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed structures to include the features now recited in Claim 1 of the instant application. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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